SSTL Based Low Power Thermal Efficient WLAN Specific 32bit ALU Design on 28nm FPGA

Kalia, Kartik; Pandey, Bishwajeet; Das, Teerath; Hussain, Dil Muhammed Akbar

Published in:
Indian Journal of Science and Technology

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

Indian Journal of Science and Technology, *Vol 9(11), DOI: 10.17485/ijst/2016/v9i11/88080, March 2016*
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

SSTL based Low Power Thermal Efficient WLAN Specific 32 bit ALU Design on 28 nm FPGA

Kalia Kartik[1*], Pandey Bishwajeet[2], Das Teerath[2] and D. M. Akbar Hussaian[3]

[1]Gyancity Research Lab, House No-3, Road No-1, South City-1 Enclave Gurgaon - 122001, India; kartikkalia4@gmail.com,
[2]GSSI, Italy; bishwajee.pandey@gssi.infn.it, teerath.das@gssi.infn.it
[3]Aalborg University, Denmark; akh@et.aau.dk

Abstract

In this paper we have designed a Thermal energy efficient 32Bit ALU for network processor, the main objective of this design is to provide better thermal efficiency with respect to existing designs. For that purpose we have used six different members of SSTL I/Os standards on 28nm technology along with consideration of airflow toward hit sink and different frequency on which ALU operate in network processor or any WLAN devices. We have done total power analysis of WLAN operating on different frequencies. We have considered a set of frequencies, which are based on IEEE 802.11 standards. First we did an analysis of IO standard on different frequencies, to find out the most efficient frequency on which device can operate at lowest power consumption and thermally efficient. Later we compared different I/Os on different frequencies, which we have considered in our paper in order to compare and find out most efficient IO standard. While analyzing we found out that when WLAN device shift from 343.15K to 283.15K, there is maximum thermal power reduction in SSTL135_R as compared to all considered I/O standards. When we compared same I/Os for different frequencies we observed maximum thermal efficiency in SSTL15 at minimum and maximum temperature as compared to all other considered I/O standards. This design has application where 32bit ALU design is considered for designing an electronic device such as WLAN. The design can be implemented on different nano chips for better efficiency depending upon the design requirement.

Keywords: 32bit ALU,28nm FPGA, Thermal Efficient,WLAN, IOs SSTL

1. Introduction

In this paper, we are going to study the most thermal efficient WLAN ALU32bit design on 28nm FPGA. WLAN is a wireless device which connects two or more devices using wireless distribution methods for example SPREAD-SPECTRUM or OFDM radio. WLAN is used within a limited area such as home, school or office area, which allows user to move around the area and still be connected to the network. Mostly WLAN's are based on IEEE 802.11 standards. We have used the following set of legally allowed WLAN channels using IEEE 802.11 protocols, mostly sold under the trade mark of wifi. How WLAN is used for multiple transmission rates[1].

Table 1. WLAN Channels.

IEEE 802.11Channels	Frequency MHz
b/g/n	2,400 MHz
y	3,600 MHz
a/h/j/n/ac	5,000 MHz
p	5,900 MHz
ad	60,000 MHz

A group of electrical standards for driving a cable

* Author for correspondence

specialized for carrying alternating current of radio frequency where wave nature must be taken into consideration for currents with high enough frequency are called SSTL. It is used with a type of random access memory that is dynamic access memory (DRAM) where each bit of data is stored in a separate capacitor in an IC (integrated circuit). This is based on double data rate (DDR) memory IC's and memory modules.

SSTL I/Os operate on different voltagesfor example SSTL18 at 1.8V, SSTL15 at 1.5V and SSTL135 at 1.35V. SSTL is supported by Artix-7 FPGA for both differential and single-ended signaling.

- **SSTL18**

SSTL18 is used for DDR2 SDRAM memory defined by the JEDEC (Joint Electron Device Engineering Council) standardJESD8-15. SSTL18_I driver supports only unidirectional technique with no bidirectional support. The SSTL18_II driver supports both unidirectional and bidirectional signaling.

- **SSTL15**

DDR3 SDRAM memory interfaces use SSTL15 IOs. It is defined by JEDEC standard JESD79-3E. SSTL15 is available in theHigh Power and High RangeI/Os banks.

SSTL15_R which is a weaker and reduced strength driver is available in High Range I/Os banks. Bidirectional and unidirectional signaling is supported by both the drivers.

- **SSTL135**

DDR3L SDRAM memory interfaces use SSTL135 IOs. It is defined by the JEDEC standard JESD79-3-1. SSTL135 which is a Full strength driver is available inHigh Power and High RangeI/Os banks.SSTL135_R is a weaker and reduced-strength driver whichis available only in the High Range I/Os banks[2].

- **Unidirectional Termination**

For SSTL15, SSTL18, SSTL135, or SSTL12 (We have not used in this paper)is shown below in the figure illustrating the sample circuit.

- **Bidirectional Termination**

For SSTL15, SSTL18, SSTL135, or SSTL12 (We have not used in this paper) is shown below in the figure illustrating the sample circuit.

We have usedHardware Description Language (HDL), Artix-7 FPGA over other FPGAs (40nm, 65nm and 90nm).

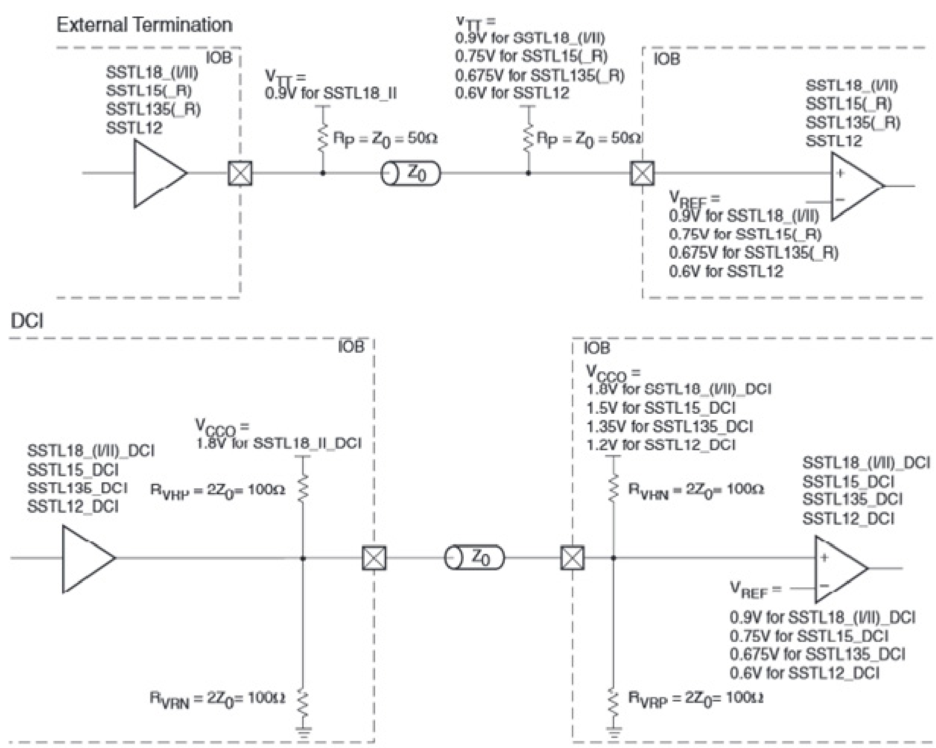

Figure 1. Unidirectional Termination.

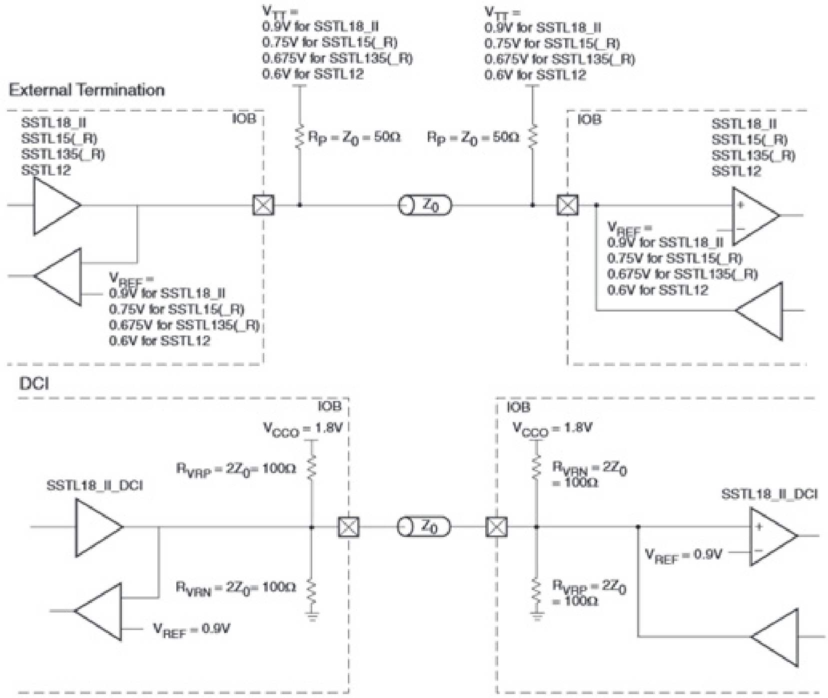

Figure 2. Bidirectional Termination.

Before 28nm there were 40nm, 65nm and 90nm but 28nm FPGA is 50% more power efficient than 40nm FPGA and has a capacity up to 2 million logic cells[3].In this paper, we are going to study the power analysis 6 different types of families of I/Os that are SSTL (STUB series terminated logic): SSTL15, SSTL15_R, SSTL18_I, SSTL18_II, SSTL135 and SSTL135_R as shown in Figure 3.

Figure 3. Different IO standards.

Here we have used 28nm (Artix-7) technology based FPGA. Our main motive is to find out most Thermal efficient I/Osfor 28nmtechnology. We have used clock gated ALU32bit circuit so as to make it more power efficient as clock gated circuit will supply power to only those lines which are important for the performance of system. How clock can be used for high performance microprocessor core in field of medical also[4].In this we have taken constant environment and only one[4] Flow of 250Linear Feet per Minute (LFM) as shown in Figure[5].

Figure 4. Airflow at 250 LFM.

- **DDR SDRAM**

Double Data Rate Synchronous Dynamic Random Access Memory. In SSTL15, SSTL18 and SSTL135 DDR is used. SSTL15 and SSTL135 use DDR3 and DDR3L whereas SSTL18 uses DDR2. DDR3L is advanced version of SDR, DDR and DDR2. DDR3L is a specially designed double data rate SDRAM which operates at low voltage 1.35V.

DDR3 is twice as efficient as DDR2 in terms of Internal rate (MHz), Prefetch (n), Data rate (MT/s), Transfer rate (GB/s) and Voltage.Methods of increasing DDR bandwidth[6].

- **ALU32bit**

Arithmetic Logical Unit and 32-bit are based on address buses, registers or data buses of that size. 32-bit register can store 2^{32} different types of values[7].

- **Applications**

WLAN is something that we use in everyday life. These are commonly known as wifi. These can be used in offices, homes or public places depending upon the availability of the device. WLAN or wifi has defined range of network within which a device can operate for example 2.4 GHz WLAN has an indoor range of up to 20 meters and a greater range outdoor. It can connect multiple devices at the same time for example laptops, mobiles, camera's or audio and video players and many more. The WLAN port or modem has an Ethernet point at back side of the device, so a user can use it via LAN wire also (Physical connection).

2. Total Power Analysis for SSTL IO Standards

We have substituted SSTL15 = S15, SSTL15_R = S15_R, SSTL18_I = S18_I, SSTL18_II = S18_II, SSTL135 = S135 and SSTL135_R = S135_R in following table.

Table 2. Power Analysis for 802.11b/g/n at 2.4 GHz.

Temp.	S15	S15_R	S18_I	S18_II	S135	S135_R
283.15K	2.279	1.304	3.661	4.328	2.227	1.282
298.15K	2.290	1.314	3.675	4.343	2.238	1.291
313.15K	2.311	1.332	3.700	4.371	2.259	1.310
328.15K	2.351	1.367	3.748	4.423	2.299	1.344
343.15K	2.421	1.429	3.831	4.512	2.369	1.407

When WLAN device shift from 343.15K to 283.15K there is 5.86%, 8.74%, 4.43%, 4.07%, 5.99% and 8.88% power reduction in SSTL15, SSTL15_R, SSTL18_I, SSTL18_II, SSTL135 and SSTL135_R respectively as shown in Table 6.

When we are using SSTL15, SSTL15_R, SSTL18_I, SSTL135 and SSTL135_R in place of SSTL18_II at 283.15k there is 47.34%, 69.87%, 15.41%, 48.54% and 70.37% respectively. At 343.15k we observe 46.34%, 68.32%, 15.09%, 47.49% and 68.81% respectively as shown in Figure 6.

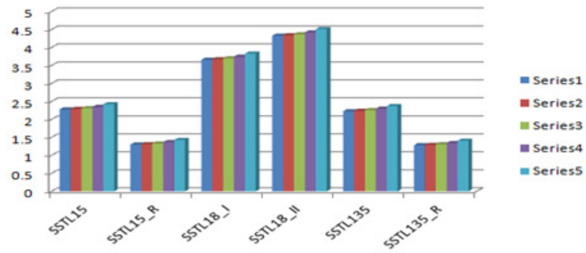

Figure 6. Total Power Analysis.

Table 3. Power analysis for 802.11y at 3.6 GHz.

Temp.	S15	S15_R	S18_I	S18_II	S135	S135_R
283.15K	3.296	1.850	5.357	6.340	3.224	1.818
298.15K	3.309	1.860	5.374	6.359	3.236	1.829
313.15K	3.334	1.880	5.406	6.396	3.260	1.849
328.15K	3.379	1.917	5.465	6.463	3.305	1.886
343.15K	3.459	1.984	5.566	6.575	3.384	1.953

When WLAN device shift from 343.15K to 283.15K, there is 4.71%, 6.75%, 3.75%, 3.57%, 4.72% and 6.91% power reduction in SSTL15, SSTL15_R, SSTL18_I, SSTL18_II, SSTL135 and SSTL135_R respectively as shown in Figure 7.

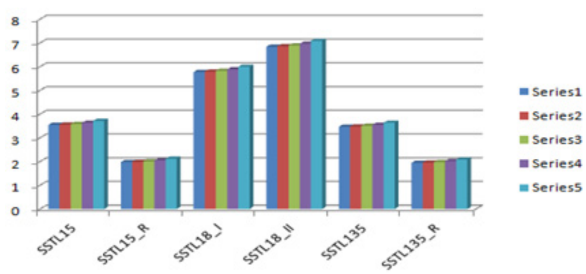

Figure 7. Total power analysis.

Table 4. Power Analysis for 802.11a/h/j/n/ac at 5.0 GHz.

Temp.	S15	S15_R	S18_I	S18_II	S135	S135_R
283.15K	4.471	2.473	7.323	8.675	4.373	2.431
298.15K	4.486	2.485	7.346	8.703	4.387	2.443
313.15K	4.514	2.506	7.338	8.753	4.416	2.464
328.15K	4.567	2.547	7.463	8.841	4.468	2.505
343.15K	4.658	2.619	7.587	8.984	4.558	2.576

When we are using SSTL15, SSTL15_R, SSTL18_I, SSTL135 and SSTL135_R in place of SSTL18_II at 283.15K there is 48.01%, 70.82%, 15.50%, 49.14% and 71.32% respectively. At 343.15k we observe 47.39%, 69.82%, 15.34%, 48.53% and 70.29% respectively as shown in Figure 7.

When WLAN device shift from 343.15K to 283.15K, there is 4.01%, 5.57%, 3.47%, 3.43%, 4.05% and 5.62% power reduction in SSTL15, SSTL15_R, SSTL18_I, SSTL18_II, SSTL135 and SSTL135_R respectively as shown in Figure 8.

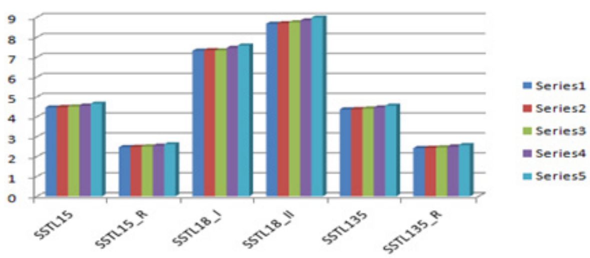

Figure 8. Total Power Analysis.

When we are using SSTL15, SSTL15_R, SSTL18_I, SSTL135 and SSTL135_R in place of SSTL18_II at 283.15k there is 48.46%, 71.49%, 15.58%, 49.59% and 71.97% respectively. At 343.15k we observe 48.15%, 70.84%, 15.54%, 48.93% and 71.32% respectively as shown in Figure 8.

Table 5. Power Analysis for 802.11p at 5.9 GHz.

Temp.	S15	S15_R	S18_I	S18_II	S135	S135_R
283.15K	*5.220*	*2.869*	*8.582*	*10.173*	*5.106*	*2.820*
298.15K	*5.237*	*2.881*	*8.602*	*10.207*	*5.122*	*2.832*
313.15K	*5.269*	*2.903*	*8.659*	*10.268*	*5.154*	*2.854*
328.15K	*5.327*	*2.946*	*8.746*	*10.371*	*5.211*	*2.897*
343.15K	*5.426*	*3.022*	*8.887*	*10.537*	*5.309*	*2.972*

When WLAN device shift from 343.15K to 283.15K there is 3.79%, 5.06%, 3.43%, 3.45%, 3.82% and 5.11% power reduction in SSTL15, SSTL15_R, SSTL18_I, SSTL18_II, SSTL135 and SSTL135_R respectively as shown in Figure 9.

When we are using SSTL15, SSTL15_R, SSTL18_I, SSTL135 and SSTL135_R in place of SSTL18_II at 283.15K there is 48.68%, 71.79%, 15.63%, 49.80% and 72.27% respectively. At 343.15K we observe 48.50%, 71.32%, 15.65%, 49.61% and 71.79% respectively as shown in Figure 9.

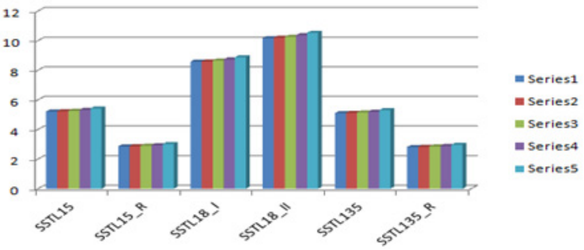

Figure 9. Total Power Analysis.

Table 6. Power analysis for 802.11ad at 60 GHz.

Temp.	S15	S15_R	S18_I	S18_II	S135	S135_R
283.15K	50.747	26.757	84.564	100.338	49.667	26.277
298.15K	50.747	26.972	84.564	100.338	49.667	26.483
313.15K	50.747	27.180	84.564	100.338	49.667	26.717
328.15K	50.747	27.180	84.564	100.388	49.667	26.717
343.15K	50.747	27.180	84.564	100.388	49.667	26.717

When WLAN device shift from 343.15K to 283.15K, there is 0%, 1.55%, 0%, 0%, 0% and 1.64% power reduction in SSTL15, SSTL15_R, SSTL18_I, SSTL18_II, SSTL135 and SSTL135_R respectively as shown in Figure 10.

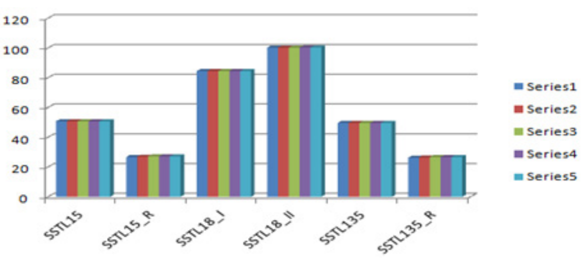

Figure 10. Total Power Analysis.

When we are using SSTL15, SSTL15_R, SSTL18_I, SSTL135 and SSTL135_R in place of SSTL18_II at 283.15K there is 49.42%, 73.33%, 15.71%, 50.50% and 73.81% respectively. At 343.15K we observe 49.42%, 72.92%, 15.54%, 48.93% and 71.38% respectively as shown in Figure 10.

3. Power Analysis for Different I/Os

When we are operating upon 2.4 GHz, 3.6 GHz, 5.0 GHz, and 5.9 GHz in place 60 GHz at 283.15k there is 95.50%, 93.50%, 91.18% and 89.71% respectively. At 343.15K we observe 95.22%, 93.18%, 90.82% and 89.30% respectively as shown in Figure 11.

Table 7. Power analysis for SSTL15 for different Freq in MHz.

Temp ↓ Freq →	2,400	3,600	5,000	5,900	60,000
283.15K	2.279	3.296	4.471	5.220	50.747
298.15K	2.290	3.309	4.486	5.237	50.747
313.15K	2.311	3.334	4.514	5.269	50.747
328.15K	2.351	3.379	4.567	5.327	50.747
343.15K	2.421	3.459	4.658	5.426	50.747

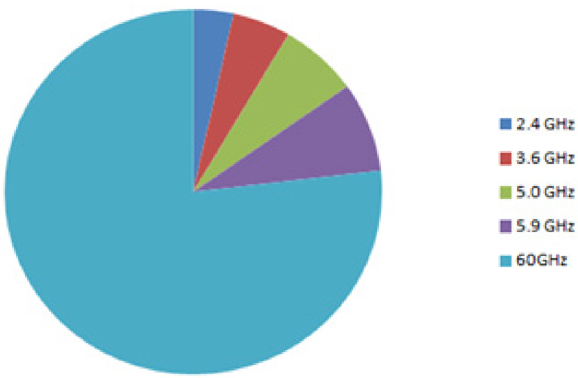

Figure 11. Power Analysis.

Table 8. Power analysis for SSTL15_R for different Freq.

Temp ↓ Freq →	2,400	3,600	5,000	5,900	60,000
283.15K	1.304	1.850	2.473	2.869	26.757
298.15K	1.314	1.860	2.485	2.881	26.972
313.15K	1.332	1.880	2.506	2.903	27.180
328.15K	1.367	1.917	2.547	2.946	27.180
343.15K	1.429	1.984	2.619	3.022	27.180

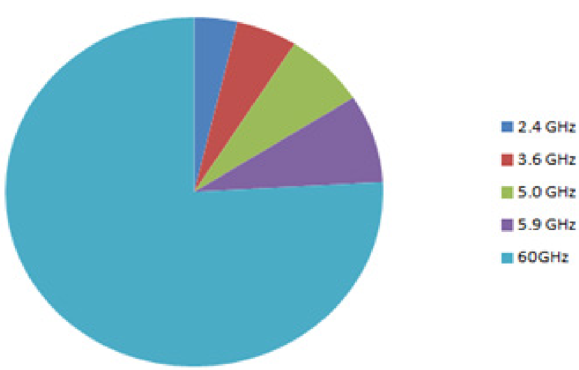

Figure 12. Power Analysis.

When we are operating upon 2.4 GHz, 3.6 GHz, 5.0 GHz, and 5.9 GHz in place 60 GHz at 283.15k there is 95.12%, 93.08%, 90.75% and 89.27% respectively. At 343.15K we observe 94.74%, 92.70%, 90.36% and 88.88% respectively as shown in Figure 12.

Table 9. Power Analysis for SSTL18_I for Different Freq.

Temp ↓ Freq →	2,400	3,600	5,000	5,900	60,000
283.15K	3.661	5.357	7.323	8.582	84.564
298.15K	3.675	5.374	7.346	8.602	84.564
313.15K	3.700	5.406	7.338	8.659	84.564
328.15K	3.748	5.465	7.463	8.746	84.564
343.15K	3.831	5.566	7.587	8.887	84.564

When we are operating upon 2.4 GHz, 3.6 GHz, 5.0 GHz, and 5.9 GHz in place 60 GHz at 283.15k there is 95.67%, 93.66%, 91.34% and 89.85% respectively. At 343.15K we observe 95.46%, 93.41%, 91.02% and 89.49% respectively as shown in Figure 13.

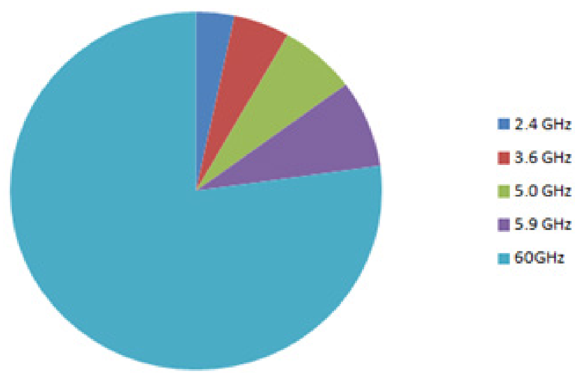

Figure 13. Power Analysis.

Table 10. Power analysis for SSTL18_II for different Freq.

Temp ↓ Freq→	2,400	3,600	5,000	5,900	60,000
283.15K	4.328	6.340	8.675	10.173	100.338
298.15K	4.343	6.359	8.703	10.207	100.338
313.15K	4.371	6.396	8.753	10.268	100.338
328.15K	4.423	6.463	8.841	10.371	100.388
343.15K	4.512	6.575	8.984	10.537	100.388

When we are operating upon 2.4 GHz, 3.6 GHz, 5.0 GHz, and 5.9 GHz in place 60 GHz at 283.15k there is 95.68%, 93.68%, 91.35% and 89.86% respectively. At

343.15K, we observe 95.50%, 93.45%, 91.05% and 89.50% respectively as shown in Figure 14.

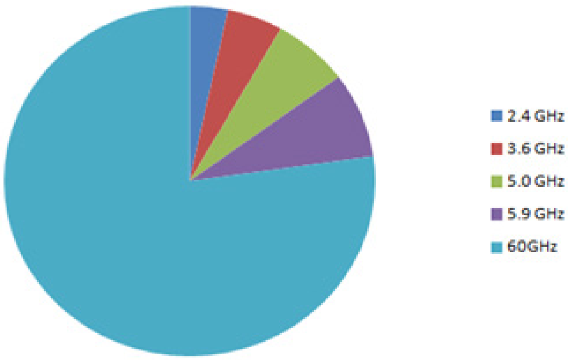

Figure 14. Power Analysis.

Table 11. Power analysis for SSTL135 for different Freq.

Temp ↓ Freq →	2,400	3,600	5,000	5,900	60,000
283.15K	2.227	3.224	4.373	5.106	49.667
298.15K	2.238	3.236	4.387	5.122	49.667
313.15K	2.259	3.260	4.416	5.154	49.667
328.15K	2.299	3.305	4.468	5.211	49.667
343.15K	2.369	3.384	4.558	5.309	49.667

When we are operating upon 2.4 GHz, 3.6 GHz, 5.0 GHz, and 5.9 GHz in place 60 GHz at 283.15k there is 95.51%, 93.50%, 91.19% and 89.66% respectively. At 343.15k we observe 94.23%, 93.18, 90.82% and 89.31% respectively as shown in Figure 15.

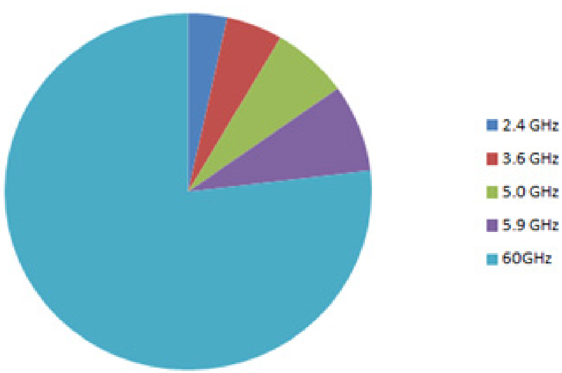

Figure 15. Power Analysis.

Table 12. Power analysis for SSTL135_R for different Freq.

Temp ↓ Freq →	2,400	3,600	5,000	5,900	60,000
283.15K	1.282	1.818	2.431	2.820	26.277
298.15K	1.291	1.829	2.443	2.832	26.483
313.15K	1.310	1.849	2.464	2.854	26.717
328.15K	1.344	1.886	2.505	2.897	26.717
343.15K	1.407	1.953	2.576	2.972	26.717

When we are operating upon 2.4 GHz, 3.6 GHz, 5.0 GHz, and 5.9 GHz in place 60 GHz at 283.15k there is 95.12%, 93.08%, 90.74% and 89.26% respectively. At 343.15K we observe 94.73%, 92.69%, 90.35% and 88.87% respectively as shown in Figure 16.

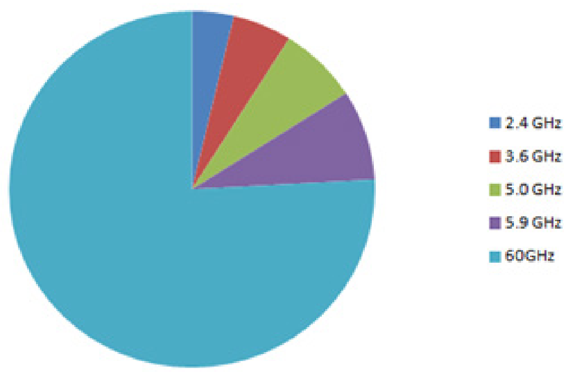

Figure 16. Power Analysis.

4. Conclusion

In order to design Thermal efficient WLAN for different channels or frequencies, When WLAN device shift from 343.15k to 283.15k there is maximum of 8.88%, 6.91%, 5.62%, 5.11% and 1.64% thermal power reduction in SSTL135_R as compared to other I/Os at 2.4 GHz, 3.6 GHz, 5.0 GHz, 5.9 GHz and 60 GHz respectively. We also observed at 60 GHz Junction temperature exceeds absolute maximum temperature for the given reading. We also observed SSTL135_R is most thermal efficient at minimum temperature 283.15K with 70.37%, 71.32%, 71.97%, 72.27% and 73.81%thermal power reduction and at maximumtemperature 343.15k there is 68.81%, 70.29%, 71.32%, 71.79% and 71.38% thermal power reduction at 2.4 GHz, 3.6 GHz, 5.0 GHz, 5.9 GHz and 60 GHz as compared to other I/Os respectively. When we compared same I/Os for different frequencies we observed at minimum temperature 283.15K, SSTL15 is most thermal efficient with 95.50%, 95.12%, 95.67%, 95.68%, 95.51% and 95.12% thermal power reduction at 2.4 GHz and at maximum temperature 343.15K there is 95.22%, 94.74%, 95.46%, 95.50%, 94.23% and 94.73% thermal power reduction at 2.4 GHz as compared to the other operating frequencies respectively.

5. Future Scope

This design is implemented on 28nm FPGA. In future, we can go forultra scale FPGA, System on Chip and 3D ICs based implementation. In this work,32bit ALU with clock gated circuit is designed for WLAN. There is an open scope to use LVTTL, LVCMOS,LVDCI, HSLVDCI, and I2C IO Standards in design of other WLAN devices. Using SSTL IO Standard, we can also design and implement Router, Microprocessors and many more WLAN device on FPGA.

6. References

1. Pavon JD Pand Choi S. Link adaptation strategy for IEEE 802. 11 WLAN via received signal strength measurement. IEEE International Conference on Communications. 2003; 2.
2. Hwang SJ and Kang KW. Input buffers and controlling methods for integrated circuit memory devices that operate with low voltage transistor-transistor logic (LVTTL) and with stub series terminated transceiver logic (SSTL). 2000 Feb1; U. S. Patent No. 6, 020, 761.
3. Chen S, XinWand Gopalan P. Xilinx next generation 28nm FPGA technology overview. Xilinx white paper: Technical report. 2010.
4. Jansen D et al. A small high performance microprocessor core sirius for embedded low power designs, demonstrated in a medical mass application of an electronic Pill. Springer US: Embedded System Design: Topics, Techniques and Trends. 2007; 363-72.
5. Hilbrink JO. Apparatus for cooling electronic devices. 1994 Aug 30; U. S. Patent No. 5, 343, 358.
6. Petersen R and SchuetteFM.Method of increasing DDR memory bandwidth in DDR SDRAM modules. 2012 Apr 3; U. S. Patent No. 8, 151, 030.
7. MetzgenP. A High Performance 32-bit ALU for Programmable Logic. ACM,Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays. 2004.